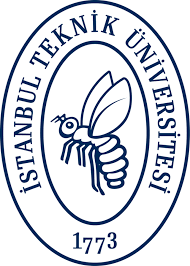
****

**DIGITAL SYSTEM DESIGN APPLICATION – EHB 436E**

**Experiment IV**

**Yiğit Bektaş GÜRSOY**

**040180063**

**Class Lecturer: Sıddıka Berna Örs Yalçın**

**Class Assistant:  
Serdar Duran  
Yasin Fırat Kula  
Mehmet Onur Demirtürk**

1. **HALF ADDER**

* Verilog Code

**module** HA**(**

**input** X**,**

**input** Y**,**

**output** COUT**,**

**output** S

**);**

**assign** COUT **=** X **&** Y**;** //CARRY

**assign** S **=** X **^** Y **;** //SUM

**endmodule**

* Testbench Code

//HALF ADDER TEST BENCH

**module** HA\_tb**();**

**reg** X**;**

**reg** Y**;**

**wire** COUT**;**

**wire** SUM**;**

HA DUT**(.**X**(**X**),**

**.**Y**(**Y**),**

**.**COUT**(**COUT**),**

**.**S**(**SUM**)**

**);**

**initial**

**begin**

X **=** 1'b0 **;** Y **=** 1'b0**;**

**#**10 X **=** 1'b0 **;** Y **=** 1'b1**;**

**#**10 X **=** 1'b1 **;** Y **=** 1'b0**;**

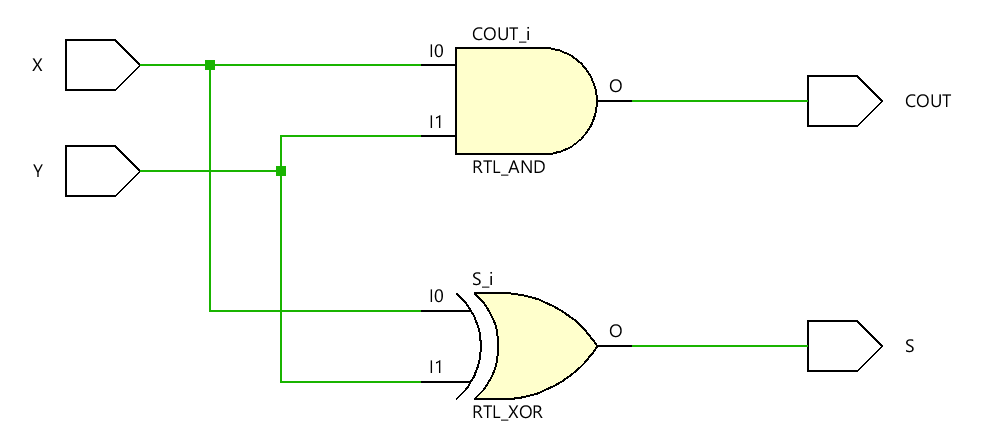
**#**10 X **=** 1'b1 **;** Y **=** 1'b1**;**

**#**10 $finish**;**

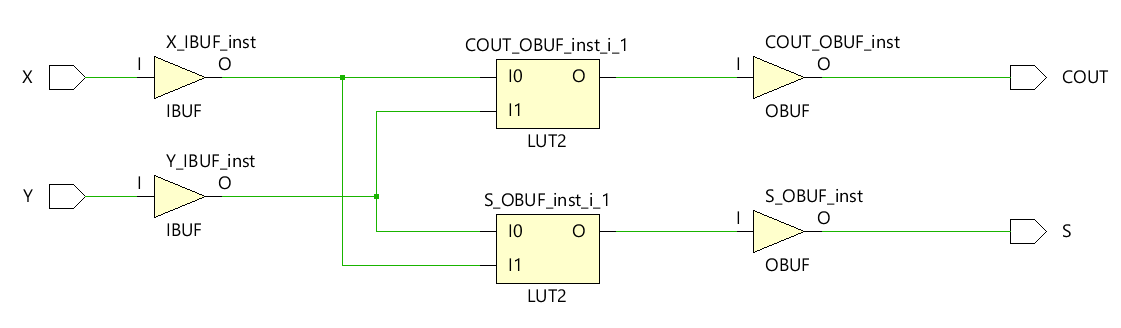
**end**

**endmodule**

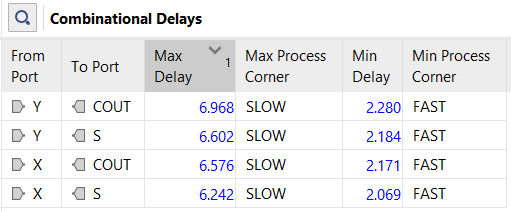
* RTL Schematic



* Technology Schematic

****

* There are 2 LUT2 in technology schematic.
* Combinational Delay

****

* The maximum delay in my circuit is 6.968ns.

1. **FULL ADDER**

* Verilog Code

**module** FA**(**

**input** X**,**

**input** Y**,**

**input** CIN**,**

**output** COUT**,**

**output** S

**);**

**wire** signal\_1**;**

**wire** signal\_2**;**

**wire** signal\_3**;**

HA halfadder1 **(** **.**X**(**X**),**

**.**Y**(**Y**),**

**.**COUT**(**signal\_1**),**

**.**S**(**signal\_2**)**

**);**

HA halfadder2 **(** **.**X**(**signal\_2**),**

**.**Y**(**CIN**),**

**.**COUT**(**signal\_3**),**

**.**S**(**S**)**

**);**

**assign** COUT **=** signal\_3 **|** signal\_1**;**

**endmodule**

* Testbench Code

//FULL ADDER TEST BENCH

**module** FA\_tb**();**

**reg** X**;**

**reg** Y**;**

**reg** CIN**;**

**wire** COUT**;**

**wire** SUM**;**

FA DUT**(.**X**(**X**),**

**.**Y**(**Y**),**

**.**CIN**(**CIN**),**

**.**COUT**(**COUT**),**

**.**S**(**SUM**)**

**);**

**initial**

**begin**

X **=** 1'b0 **;** Y **=** 1'b0**;** CIN **=** 1'b0**;**

**#**10 X **=** 1'b0 **;** Y **=** 1'b0**;** CIN **=** 1'b1**;**

**#**10 X **=** 1'b0 **;** Y **=** 1'b1**;** CIN **=** 1'b0**;**

**#**10 X **=** 1'b0 **;** Y **=** 1'b1**;** CIN **=** 1'b1**;**

**#**10 X **=** 1'b1 **;** Y **=** 1'b0**;** CIN **=** 1'b0**;**

**#**10 X **=** 1'b1 **;** Y **=** 1'b0**;** CIN **=** 1'b1**;**

**#**10 X **=** 1'b1 **;** Y **=** 1'b1**;** CIN **=** 1'b0**;**

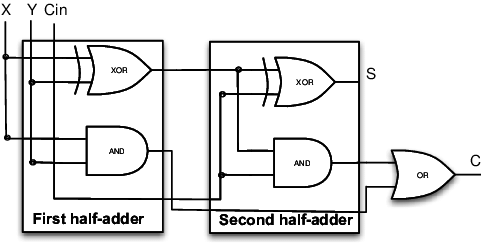
**#**10 X **=** 1'b1 **;** Y **=** 1'b1**;** CIN **=** 1'b1**;**

**#**10 $finish**;**

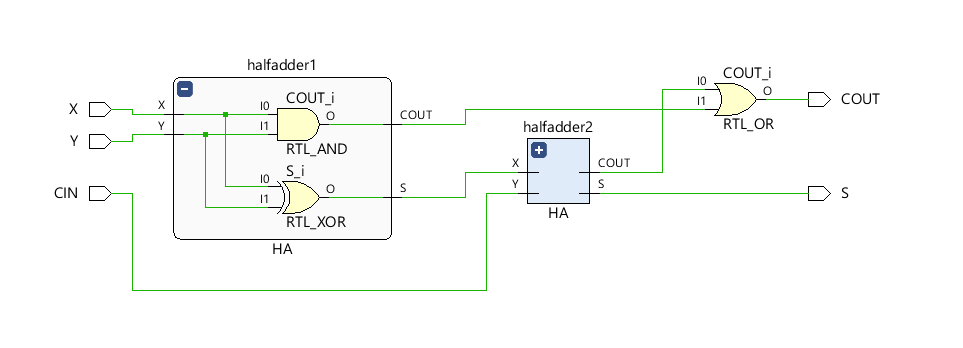
**end**

**endmodule**

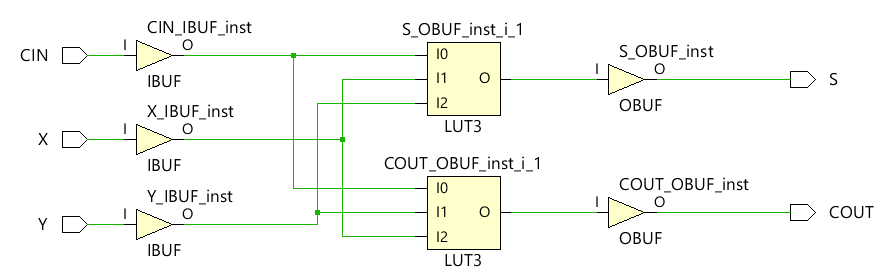
* Full-adder Circuit



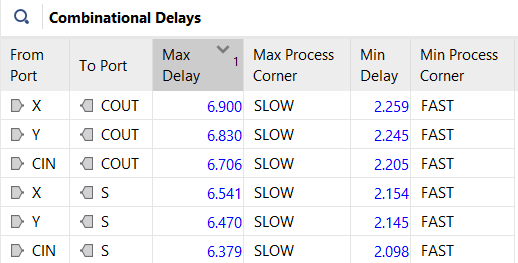
* RTL Schematic

****

* Technology Schematic

****

* There are 2 LUT3 in technology schematic.
* Combinational Delay



* The maximum delay in my circuit is 6.9ns.

1. **RIPPLE CARRY ADDER**

* Verilog Code

**module** RCA**(**

**input** **[**3**:**0**]**X**,**

**input** **[**3**:**0**]**Y**,**

**input** CIN**,**

**output** COUT**,**

**output** **[**3**:**0**]**S

**);**

**wire** c1**,**c2**,**c3**,**c4**;**

FA fulladder1**(**

**.**X**(**X**[**0**]),**

**.**Y**(**Y**[**0**]),**

**.**CIN**(**CIN**),**

**.**COUT**(**c1**),**

**.**S**(**S**[**0**])**

**);**

FA fulladder2**(**

**.**X**(**X**[**1**]),**

**.**Y**(**Y**[**1**]),**

**.**CIN**(**c1**),**

**.**COUT**(**c2**),**

**.**S**(**S**[**1**])**

**);**

FA fulladder3**(**

**.**X**(**X**[**2**]),**

**.**Y**(**Y**[**2**]),**

**.**CIN**(**c2**),**

**.**COUT**(**c3**),**

**.**S**(**S**[**2**])**

**);**

FA fulladder4**(**

**.**X**(**X**[**3**]),**

**.**Y**(**Y**[**3**]),**

**.**CIN**(**c3**),**

**.**COUT**(**COUT**),**

**.**S**(**S**[**3**])**

**);**

**endmodule**

* Testbench Code

//RIPPLE CARRY ADDER TEST BENCH

**module** RCA\_tb**();**

**reg** **[**3**:**0**]**X**;**

**reg** **[**3**:**0**]**Y**;**

**reg** CIN**;**

**wire** COUT**;**

**wire** **[**3**:**0**]**SUM**;**

RCA DUT**(.**X**(**X**),**

**.**Y**(**Y**),**

**.**CIN**(**CIN**),**

**.**COUT**(**COUT**),**

**.**S**(**SUM**)**

**);**

**initial**

**begin**

X **=** 4'b0000 **;** Y **=** 4'b0000**;** CIN **=** 1'b0**;**

**#**10 X **=** 4'b1110 **;** Y **=** 4'b0011**;** CIN **=** 1'b1**;**

**#**10 X **=** 4'b0110 **;** Y **=** 4'b1100**;** CIN **=** 1'b0**;**

**#**10 X **=** 4'b0011 **;** Y **=** 4'b1010**;** CIN **=** 1'b1**;**

**#**10 X **=** 4'b1000 **;** Y **=** 4'b1111**;** CIN **=** 1'b0**;**

**#**10 X **=** 4'b1111 **;** Y **=** 4'b0101**;** CIN **=** 1'b1**;**

**#**10 X **=** 4'b1001 **;** Y **=** 4'b1100**;** CIN **=** 1'b0**;**

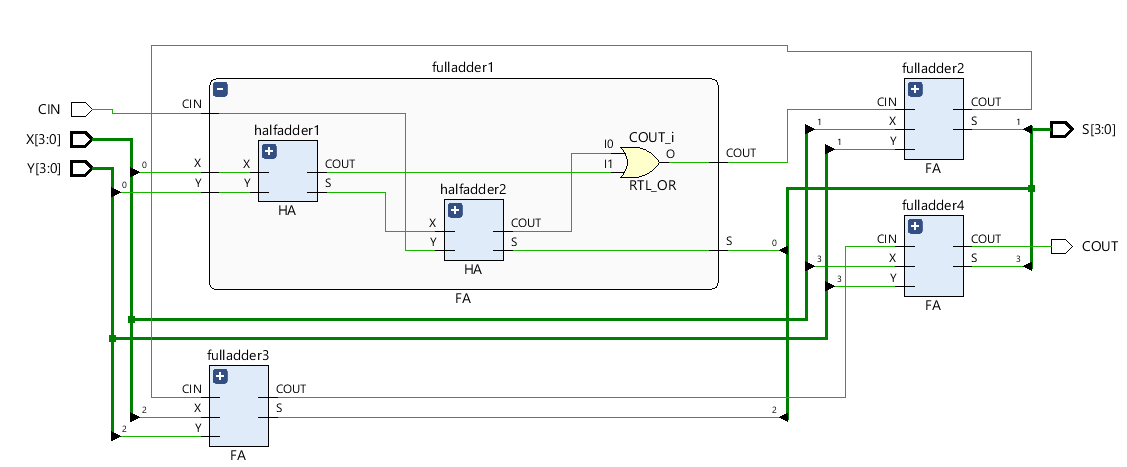
**#**10 X **=** 4'b1101 **;** Y **=** 4'b1111**;** CIN **=** 1'b1**;**

**#**10 $finish**;**

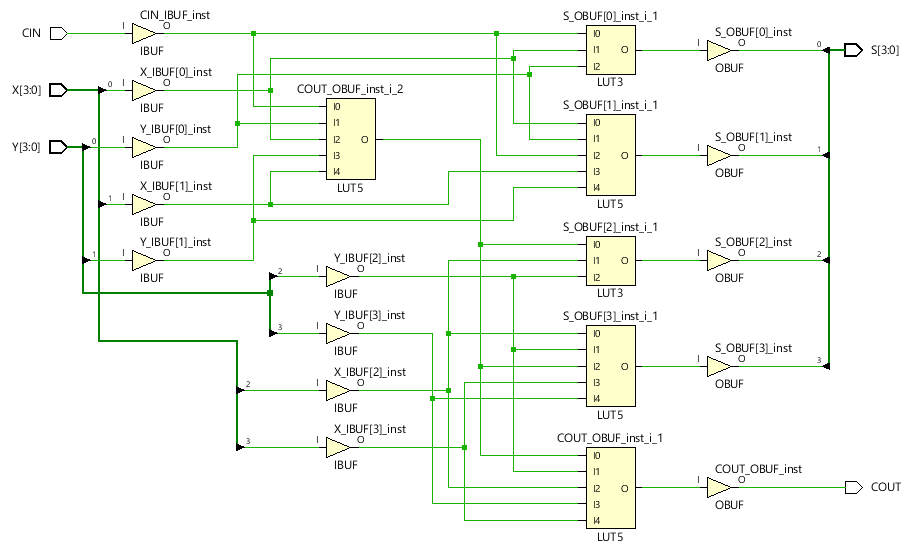
**end**

**endmodule**

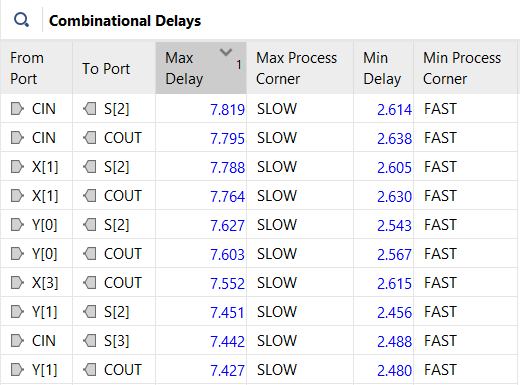
* RTL Schematic



* Technology Schematic

****

* There are 4 LUT5 and 2 LUT3 in technology schematic.
* Combinational Delay

****

* The maximum delay in my circuit is 7.819ns.

1. **RIPPLE CARRY ADDER WITH GENERATE FOR**

* Verilog Code

**module** parametric\_RCA **#(** **parameter** SIZE**=**4 **)**

**(**

**input** **[**SIZE**-**1**:**0**]**X**,**

**input** **[**SIZE**-**1**:**0**]**Y**,**

**input** CIN**,**

**output** COUT**,**

**output** **[**SIZE**-**1**:**0**]**S

**);**

**wire** **[**SIZE**:**0**]**signal**;**

**assign** signal**[**0**]** **=** CIN**;**

**genvar** i**;**

**generate**

**for(**i **=** 0**;** i **<** SIZE**;** i **=** i **+** 1**)**

**begin:** generated\_FA

FA fulladder**(**

X**[**i**],**

Y**[**i**],**

signal**[**i**],**

signal**[**i**+**1**],**

S**[**i**]**

**);**

**end**

**endgenerate**

**assign** COUT **=** signal**[**SIZE**];**

**endmodule**

* 4-bit wide Testbench Code

**module** parametric\_RCA\_tb**();**

**parameter** SIZE **=** 4 **;**

**reg** **[**SIZE**-**1**:**0**]**X**;**

**reg** **[**SIZE**-**1**:**0**]**Y**;**

**reg** CIN**;**

**wire** COUT**;**

**wire** **[**SIZE**-**1**:**0**]**S**;**

parametric\_RCA **#(**

**.**SIZE**(**SIZE**)**

**)**

RCA1**(.**X**(**X**),**

**.**Y**(**Y**),**

**.**CIN**(**CIN**),**

**.**COUT**(**COUT**),**

**.**S**(**S**));**

**initial**

**begin**

X **=** 4'b0011 **;** Y **=** 4'b0011**;** CIN **=** 1'b1**;**

**#**10 X **=** 4'b0110 **;** Y **=** 4'b1000**;** CIN **=** 1'b0**;**

**#**10 X **=** 4'b0011 **;** Y **=** 4'b1000**;** CIN **=** 1'b1**;**

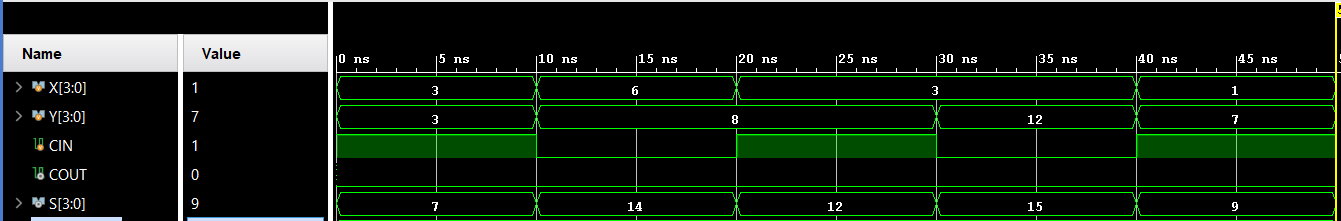
**#**10 X **=** 4'b0011 **;** Y **=** 4'b1100**;** CIN **=** 1'b0**;**

**#**10 X **=** 4'b0001 **;** Y **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 $finish**;**

**end**

**endmodule**

* ****4-bit wide simulation result
* 8-bit wide testbench code

**module** parametric\_RCA\_tb**();**

**parameter** SIZE **=** 4 **;**

**reg** **[**SIZE**-**1**:**0**]**X**;**

**reg** **[**SIZE**-**1**:**0**]**Y**;**

**reg** CIN**;**

**wire** COUT**;**

**wire** **[**SIZE**-**1**:**0**]**S**;**

parametric\_RCA **#(**

**.**SIZE**(**SIZE**)**

**)**

RCA1**(.**X**(**X**),**

**.**Y**(**Y**),**

**.**CIN**(**CIN**),**

**.**COUT**(**COUT**),**

**.**S**(**S**));**

**initial**

**begin**

X **=** 8'b10001110 **;** Y **=** 8'b10100011**;** CIN **=** 1'b1**;**

**#**10 X **=** 8'b01010110 **;** Y **=** 8'b00111100**;** CIN **=** 1'b0**;**

**#**10 X **=** 8'b01100011 **;** Y **=** 8'b10001010**;** CIN **=** 1'b1**;**

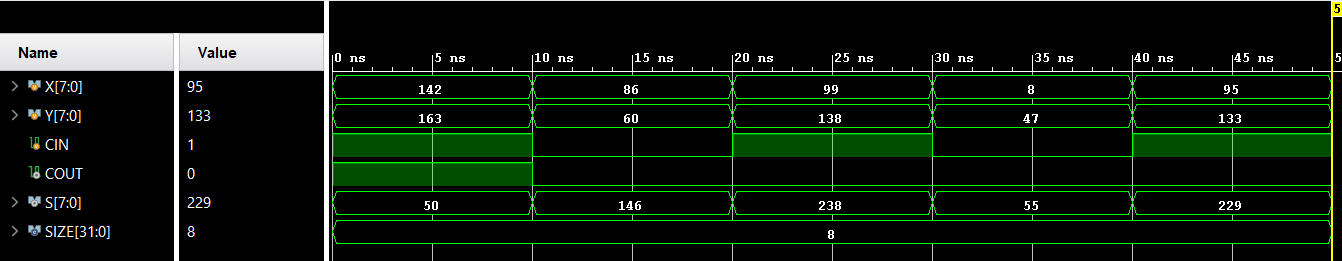
**#**10 X **=** 8'b00001000 **;** Y **=** 8'b00101111**;** CIN **=** 1'b0**;**

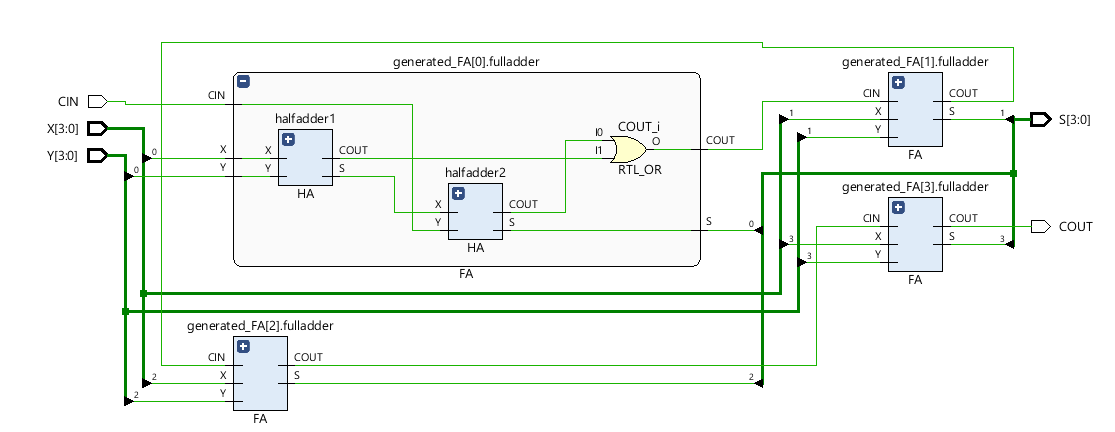
**#**10 X **=** 8'b01011111 **;** Y **=** 8'b10000101**;** CIN **=** 1'b1**;**

**#**10 $finish**;**

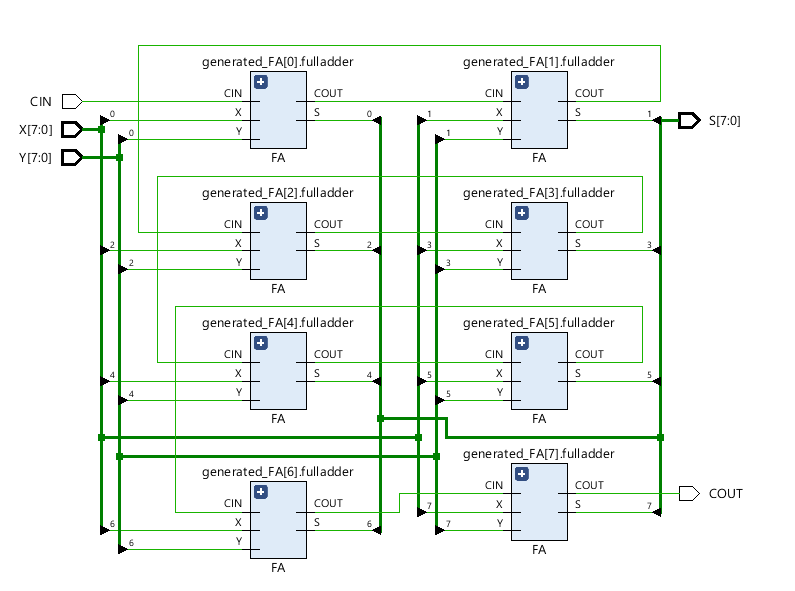
**end**

**endmodule**

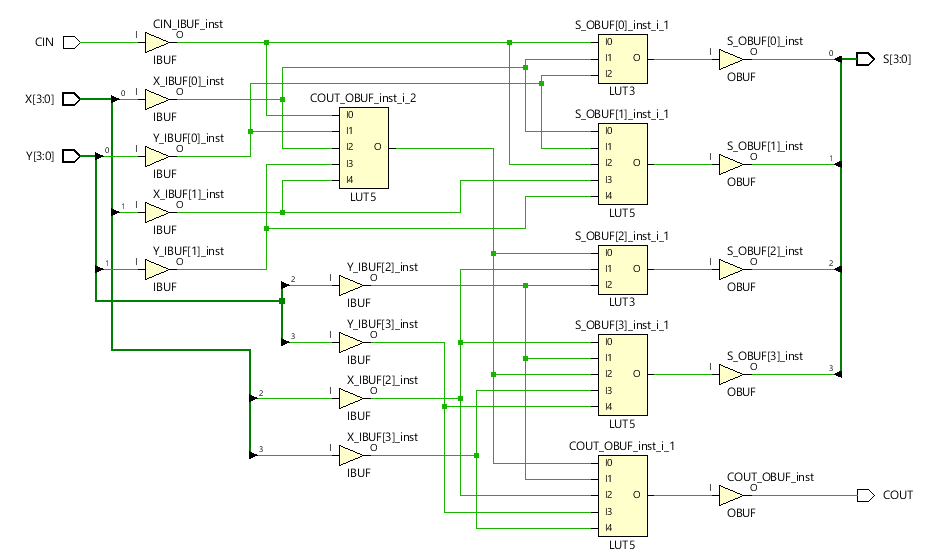
* ****8-bit wide simulation result
* RTL Schematic
* 4-bit wide RCA with generate for

****

* 8-bit wide RCA with generate for

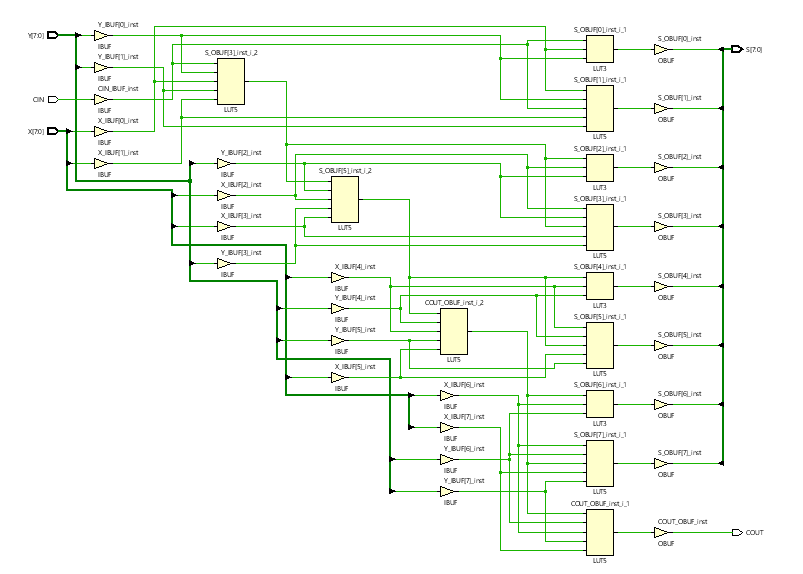
****

* Technology Schematic
* 4-bit wide RCA with generate for

****

4-bit wide RCA with generate for includes 4 LUT5s and 2 LUT3.

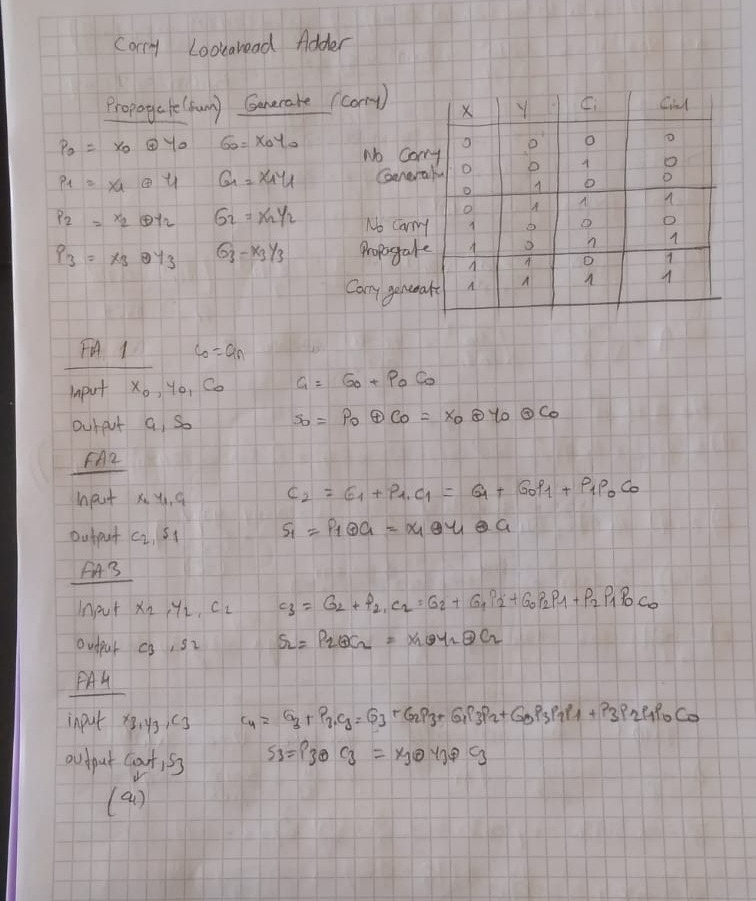
* 8-bit wide RCA with generate for



8-bit wide RCA with generate for includes 8 LUT5s and 3 LUT3.

Our 4-bit RCA circuits are very similar to each other. In our 8-bit RCA circuit, the use of LUT5 and LUT3 is more.

1. **CARRY LOOKAHEAD ADDER**



* Verilog Code

**module** CGA **(** //carry , generate , propagate

**input** **[**3**:**0**]**P**,**

**input** **[**3**:**0**]**G**,**

**input** CIN**,**

**output** **[**3**:**0**]**COUT

**);**

**assign** COUT**[**0**]** **=** G**[**0**]** **|** **(**P**[**0**]** **&** CIN**);**

**assign** COUT**[**1**]** **=** G**[**1**]** **|** **(**G**[**0**]** **&** P**[**1**])** **|** **(**P**[**1**]** **&** P**[**0**]** **&** CIN**);**

**assign** COUT**[**2**]** **=** G**[**2**]** **|** **(**G**[**1**]** **&** P**[**2**])** **|** **(**G**[**0**]** **&** P**[**2**]** **&** P**[**1**])** **|** **(** P**[**2**]** **&** P**[**1**]** **&** P**[**0**]** **&** CIN**);**

**assign** COUT**[**3**]** **=** G**[**3**]** **|** **(**G**[**2**]** **&** P**[**3**])** **|** **(**G**[**1**]** **&** P**[**3**]** **&** P**[**2**])** **|** **(**G**[**0**]** **&** P**[**3**]** **&** P**[**2**]** **&** P**[**1**])** **|** **(**P**[**3**]** **&** P**[**2**]** **&** P**[**1**]** **&** P**[**0**]** **&** CIN**);**

**endmodule**

**module** CLA **(**

**input** **[**3**:**0**]**X**,**

**input** **[**3**:**0**]**Y**,**

**input** CIN**,**

**output** COUT**,**

**output** **[**3**:**0**]**S

**);**

**wire** **[**3**:**0**]**P**;**

**wire** **[**3**:**0**]**G**;**

**wire** **[**3**:**0**]**C**;**

**assign** P **=** X **^** Y**;**

**assign** G **=** X **&** Y**;**

CGA CGA**(**

**.**P**(**P**),**

**.**G**(**G**),**

**.**CIN**(**CIN**),**

**.**COUT**(**C**)**

**);**

**assign** COUT **=** C**[**3**];**

**assign** S**[**0**]** **=** P**[**0**]** **^** CIN**;**

**assign** S**[**1**]** **=** P**[**1**]** **^** C**[**0**];**

**assign** S**[**2**]** **=** P**[**2**]** **^** C**[**1**];**

**assign** S**[**3**]** **=** P**[**3**]** **^** C**[**2**];**

**endmodule**

* Testbench Code

//CLA TEST BENCH

**module** CLA\_tb**();**

**reg** **[**3**:**0**]**X**;**

**reg** **[**3**:**0**]**Y**;**

**reg** CIN**;**

**wire** COUT**;**

**wire** **[**3**:**0**]**S**;**

CLA DUT**(.**X**(**X**),**

**.**Y**(**Y**),**

**.**CIN**(**CIN**),**

**.**COUT**(**COUT**),**

**.**S**(**S**)**

**);**

**initial**

**begin**

X **=** 4'b0000 **;** Y **=** 4'b0000**;** CIN **=** 1'b0**;**

**#**10 X **=** 4'b1110 **;** Y **=** 4'b0011**;** CIN **=** 1'b1**;**

**#**10 X **=** 4'b0110 **;** Y **=** 4'b1100**;** CIN **=** 1'b0**;**

**#**10 X **=** 4'b0011 **;** Y **=** 4'b1010**;** CIN **=** 1'b1**;**

**#**10 X **=** 4'b1000 **;** Y **=** 4'b1111**;** CIN **=** 1'b0**;**

**#**10 X **=** 4'b1111 **;** Y **=** 4'b0101**;** CIN **=** 1'b1**;**

**#**10 X **=** 4'b1001 **;** Y **=** 4'b1100**;** CIN **=** 1'b0**;**

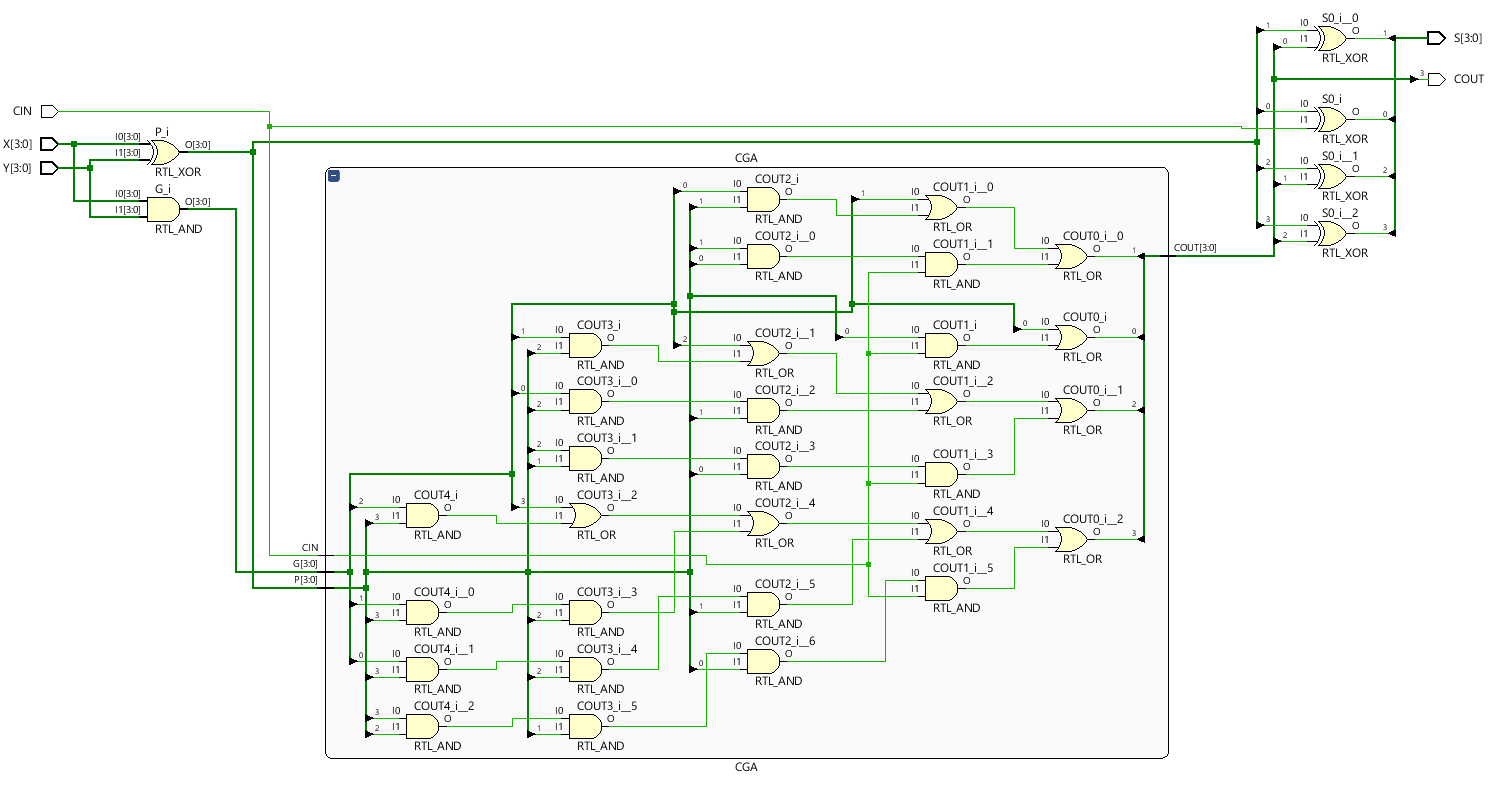
**#**10 X **=** 4'b1101 **;** Y **=** 4'b1111**;** CIN **=** 1'b1**;**

**#**10 $finish**;**

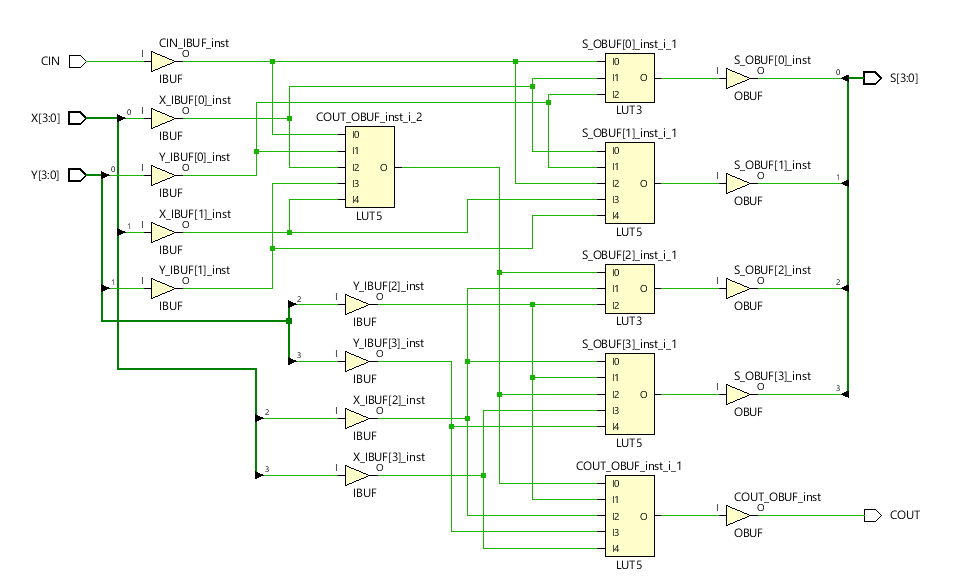
**end**

**endmodule**

* RTL Schematic

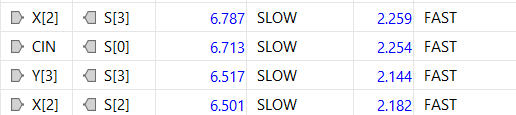
****

* Technology Schematic



* There are 2 LUT3 and 4 LUT5 in technology schematic.
* Combinational Delay





* The maximum delay in my circuit is 7.819ns. We can say that most of the combinational delays are either close to 7ns or higher than 7ns.

1. **ADDER-SUBSTRACTOR CIRCUIT WITH OVERFLOW DETECTION**

* Verilog Code

**module** ADD\_SUB

**(**

**input** **[**3**:**0**]**A**,**

**input** **[**3**:**0**]**B**,**

**input** CIN**,**

**output** **[**3**:**0**]**SUM**,**

**output** COUT**,**

**output** V

**);**

**wire** fa1\_in**,** fa2\_in**,** fa3\_in**,** fa4\_in**;**

**wire** fa1\_cout**,** fa2\_cout**,** fa3\_cout**;**

**assign** fa1\_in **=** CIN **^** B**[**0**];**

**assign** fa2\_in **=** CIN **^** B**[**1**];**

**assign** fa3\_in **=** CIN **^** B**[**2**];**

**assign** fa4\_in **=** CIN **^** B**[**3**];**

FA FA1

**(**

**.**X**(**A**[**0**]),**

**.**Y**(**fa1\_in**),**

**.**CIN**(**CIN**),**

**.**COUT**(**fa1\_cout**),**

**.**S**(**SUM**[**0**])**

**);**

FA FA2

**(**

**.**X**(**A**[**1**]),**

**.**Y**(**fa2\_in**),**

**.**CIN**(**fa1\_cout**),**

**.**COUT**(**fa2\_cout**),**

**.**S**(**SUM**[**1**])**

**);**

FA FA3

**(**

**.**X**(**A**[**2**]),**

**.**Y**(**fa3\_in**),**

**.**CIN**(**fa2\_cout**),**

**.**COUT**(**fa3\_cout**),**

**.**S**(**SUM**[**2**])**

**);**

FA FA4

**(**

**.**X**(**A**[**3**]),**

**.**Y**(**fa4\_in**),**

**.**CIN**(**fa3\_cout**),**

**.**COUT**(**COUT**),**

**.**S**(**SUM**[**3**])**

**);**

**assign** V **=** fa3\_cout **^** COUT**;**

**endmodule**

* Testbench Code

**module** ADD\_SUB\_tb**();**

**reg** **[**3**:**0**]**A**;**

**reg** **[**3**:**0**]**B**;**

**reg** CIN**;**

**wire** COUT**;**

**wire** V**;**

**wire** **[**3**:**0**]** SUM**;**

ADD\_SUB AS

**(**

**.**A**(**A**),**

**.**B**(**B**),**

**.**CIN**(**CIN**),**

**.**COUT**(**COUT**),**

**.**V**(**V**),**

**.**SUM**(**SUM**)**

**);**

**initial**

**begin**

A **=** 4'b0000**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b0001**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b0010**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b0011**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b0100**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b0101**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b0110**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b0111**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b1000**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b1001**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b1010**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b1011**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b1100**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b1101**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b1110**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b1111**;** B **=** 4'b0111**;** CIN **=** 1'b0**;**

**#**10 A **=** 4'b0000**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b0001**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b0010**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b0011**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b0100**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b0101**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b0110**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b0111**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b1000**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b1001**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b1010**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b1011**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b1100**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

**#**10 A **=** 4'b1101**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

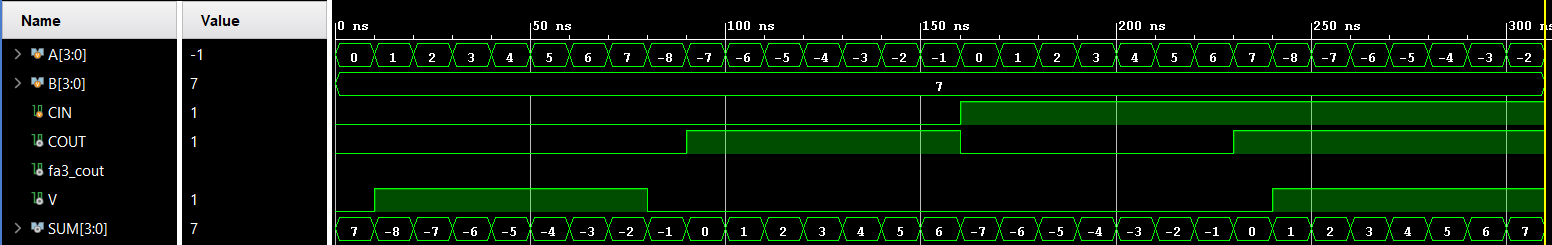
**#**10 A **=** 4'b1110**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

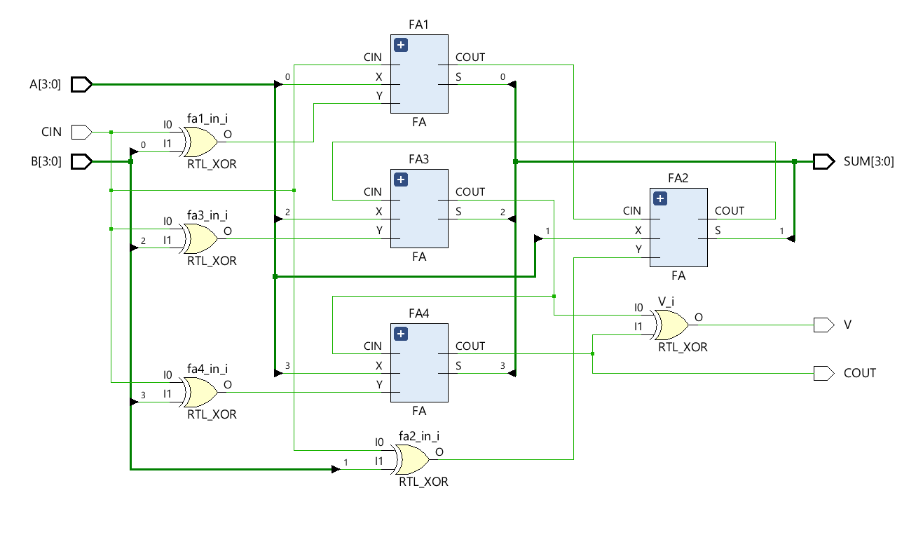
**#**10 A **=** 4'b1111**;** B **=** 4'b0111**;** CIN **=** 1'b1**;**

$finish**;**

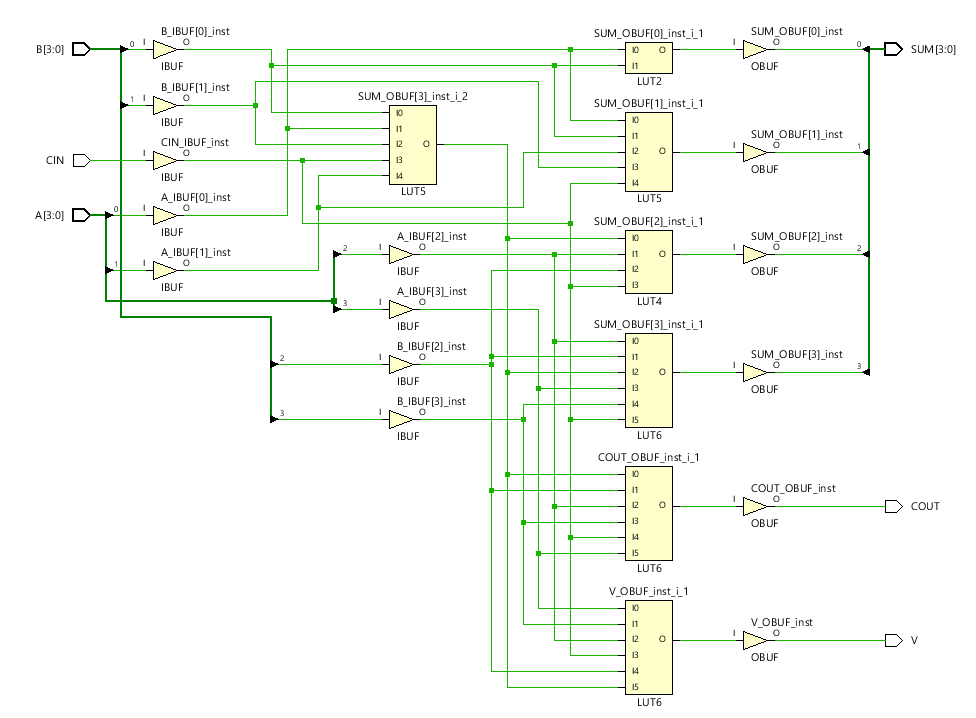
**end**

**endmodule**

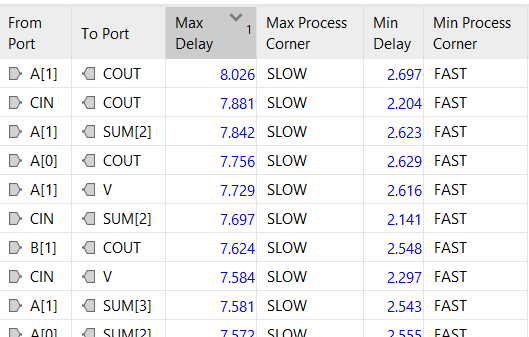
* Behavioral Simulation
* The values representing the yields at the outputs of the 3rd and 4th Full adders are fa3\_cout and COUT, respectively.
* RTL Schematic



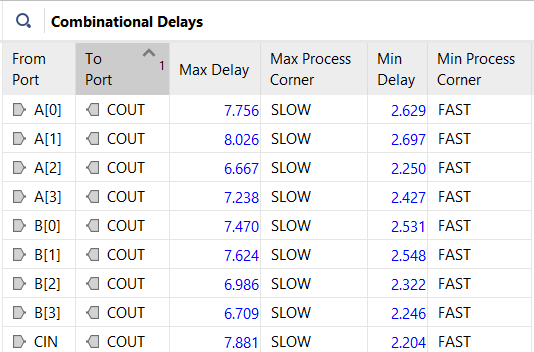
* Technology Schematic



* There are 1 LUT2, 1 LUT4, 2 LUT5 and 3 LUT6 in technology schematic.
* Combinational Delay



* The maximum delay in my circuit is 8.026ns



* In the photo above, the delays are arranged according to the output COUT. Delays are usually between 7ns and 8ns.

1. **RCA AND CLA COMPARISON WITH DONT TOUCH STRUCTURE ( OPTIONAL)**

* Our results with our max delays were supposed to have less delay in terms of coding and structure in CLA, but since our program did its own optimization, the delays were equal in both cases. If we give the structure (\*dont \_touch = "true"\*) to the wire parts, we can find the differences between them.
* Verilog Code (RCA and CLA)

**module** CGA **(** //carry , generate , propagate

**input** **[**3**:**0**]**P**,**

**input** **[**3**:**0**]**G**,**

**input** CIN**,**

**output** **[**3**:**0**]**COUT

**);**

**assign** COUT**[**0**]** **=** G**[**0**]** **|** **(**P**[**0**]** **&** CIN**);**

**assign** COUT**[**1**]** **=** G**[**1**]** **|** **(**G**[**0**]** **&** P**[**1**])** **|** **(**P**[**1**]** **&** P**[**0**]** **&** CIN**);**

**assign** COUT**[**2**]** **=** G**[**2**]** **|** **(**G**[**1**]** **&** P**[**2**])** **|** **(**G**[**0**]** **&** P**[**2**]** **&** P**[**1**])** **|** **(** P**[**2**]** **&** P**[**1**]** **&** P**[**0**]** **&** CIN**);**

**assign** COUT**[**3**]** **=** G**[**3**]** **|** **(**G**[**2**]** **&** P**[**3**])** **|** **(**G**[**1**]** **&** P**[**3**]** **&** P**[**2**])** **|** **(**G**[**0**]** **&** P**[**3**]** **&** P**[**2**]** **&** P**[**1**])** **|** **(**P**[**3**]** **&** P**[**2**]** **&** P**[**1**]** **&** P**[**0**]** **&** CIN**);**

**endmodule**

**module** CLA **(**

**input** **[**3**:**0**]**X**,**

**input** **[**3**:**0**]**Y**,**

**input** CIN**,**

**output** COUT**,**

**output** **[**3**:**0**]**S

**);**

**(\*** dont\_touch **=** "true" **\*)** **wire** **[**3**:**0**]**P**;**

**(\*** dont\_touch **=** "true" **\*)** **wire** **[**3**:**0**]**G**;**

**(\*** dont\_touch **=** "true" **\*)** **wire** **[**3**:**0**]**C**;**

**assign** P **=** X **^** Y**;**

**assign** G **=** X **&** Y**;**

CGA CGA**(**

**.**P**(**P**),**

**.**G**(**G**),**

**.**CIN**(**CIN**),**

**.**COUT**(**C**)**

**);**

**assign** COUT **=** C**[**3**];**

**assign** S**[**0**]** **=** P**[**0**]** **^** CIN**;**

**assign** S**[**1**]** **=** P**[**1**]** **^** C**[**0**];**

**assign** S**[**2**]** **=** P**[**2**]** **^** C**[**1**];**

**assign** S**[**3**]** **=** P**[**3**]** **^** C**[**2**];**

**endmodule**

**module** RCA**(**

**input** **[**3**:**0**]**X**,**

**input** **[**3**:**0**]**Y**,**

**input** CIN**,**

**output** COUT**,**

**output** **[**3**:**0**]**S

**);**

**(\*** dont\_touch **=** "true" **\*)wire** c1**,**c2**,**c3**,**c4**;**

FA fulladder1**(**

**.**X**(**X**[**0**]),**

**.**Y**(**Y**[**0**]),**

**.**CIN**(**CIN**),**

**.**COUT**(**c1**),**

**.**S**(**S**[**0**])**

**);**

FA fulladder2**(**

**.**X**(**X**[**1**]),**

**.**Y**(**Y**[**1**]),**

**.**CIN**(**c1**),**

**.**COUT**(**c2**),**

**.**S**(**S**[**1**])**

**);**

FA fulladder3**(**

**.**X**(**X**[**2**]),**

**.**Y**(**Y**[**2**]),**

**.**CIN**(**c2**),**

**.**COUT**(**c3**),**

**.**S**(**S**[**2**])**

**);**

FA fulladder4**(**

**.**X**(**X**[**3**]),**

**.**Y**(**Y**[**3**]),**

**.**CIN**(**c3**),**

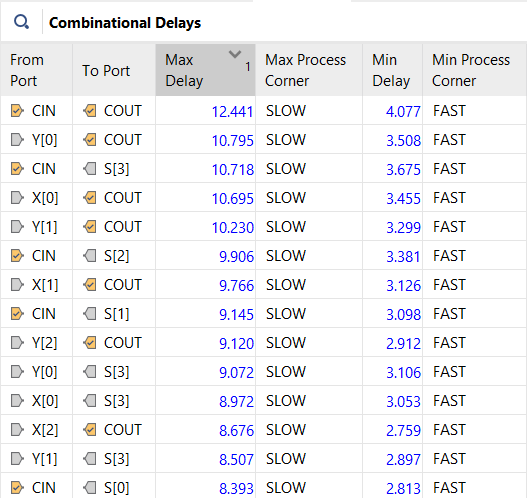
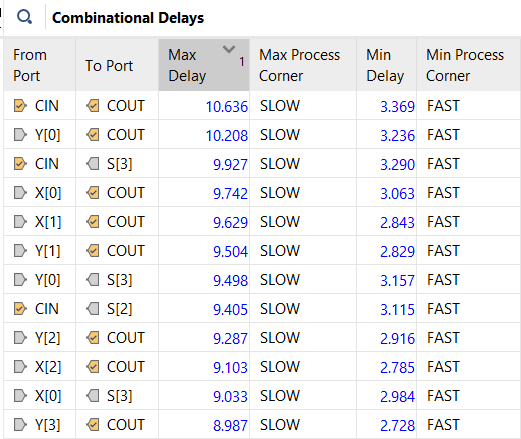
**.**COUT**(**COUT**),**

**.**S**(**S**[**3**])**

**);**

**endmodule**

* Combinational Delay



**RCA DELAY WITH DONT\_TOUCH**

**CLA DELAY WITH DONT\_TOUCH**

* As you can see, the max delay in the RCA module that we made with the dont\_touch structure was 12,441 ns, and the max delay in the CLA module was 10.636ns. There is a difference of about 2ns between them. Although both are summation circuits, the CLA module works faster than the RCA module. This is due to its design.